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04545094 E.I. No: EIP96110399120
Title: Two-dimensional optical **star-network**
Author: Danzer, U.; Schwider, J.
Corporate Source: Universitaet Erlangen-Nuernberg, Erlangen, Ger
Conference Title: Proceedings of the 1996 Conference on Lasers and Electro-Optics Europe, CLEO/Europe
Conference Location: Hamburg, Ger Conference Date: 19960908-19960913
Sponsor: European Physical Society; Quantum Electronics & Optics Division ; IEEE/LEOS; Optical Society of America; Eur Optical Society
E.I. Conference No.: 45465
Source: Conference on Lasers and Electro-Optics Europe - Technical Digest 1996.. p 276 CThI50
Publication Year: 1996
CODEN: 85PNA9
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9612W5
Abstract: An interconnection network for a modular expandable multiprocessor system is shown. Such a **computer system** needs a direct **coupling** among all **processor** units. For synchronization purposes or **clock** distribution the signal delay from one transmitter to all receivers should be the same. A fiber **optical** star network ensures a data distribution from all emitters to all receivers without delay, assuming equal fiber lengths. For this application, a star-topology bus system (STBS) has been developed. 2 Refs.
Descriptors: Fiber optic networks; Fiber optics; Diffraction gratings; Electric network topology; Transmitters; Signal receivers; **Optical** fiber coupling; Optoelectronic devices; Interconnection networks; **Optical** beam splitters
Identifiers: **Optical** star network; Star topology bus system; Free space **optical** setup; Wavelength
Classification Codes:
741.1.2 (Fiber Optics)
741.1 (Light/Optics); 741.3 (Optical Devices & Systems); 716.1 (Information & Communication Theory); 717.2 (Optical Communication Equipment); 722.4 (Digital Computers & Systems)
741 (Optics & Optical Devices); 716 (Radar, Radio & TV Electronic Equipment); 717 (Electro-Optical Communications); 722 (Computer Hardware)
74 (OPTICAL TECHNOLOGY); 71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

12/9/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03741413 **Image available**
CONTROLLER FOR ASTRONOMICAL TELESCOPE

PUB. NO.: 04-106513 [JP 4106513 A]
PUBLISHED: April 08, 1992 (**19920408**)
INVENTOR(s): YAMAMOTO SEIICHI
APPLICANT(s): WAAPU KURIEITO SHISUTEMUZU KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-225681 [JP 90225681]
FILED: August 27, 1990 (19900827)
INTL CLASS: [5] G02B-023/00
JAPIO CLASS: 29.2 (PRECISION INSTRUMENTS -- **Optical** Equipment)
JOURNAL: Section: P, Section No. 1393, Vol. 16, No. 348, Pg. 74, July

28, 1992 (19920728)

ABSTRACT

PURPOSE: To easily and rapidly bring a desired celestial body in an astronomical telescope by inputting the desired observed celestial body which is to be observed, obtaining the present coordinate of the designated observed celestial body and turning the astronomical telescope to the present coordinate which is obtained.

CONSTITUTION: This controller 1 for the astronomical telescope is provided with the astronomical telescope 3, a driving **device** 5, a control **computer** 7 and a **display** 9. A **clock** device 11 and a handset 13 are **connected** to the device 5. Then, the controller 1 designates the desired celestial body by a star chart and a celestial menu **displayed** on the **display** 9 or it designates the coordinate value of desired right ascension and declination, so that the telescope 3 is brought to be in the state of the desired celestial body and the coordinate of the desired right ascension and declination. After fixing the value of the right ascension and declination, the telescope 3 is turned in a designated direction and the celestial body of visual field is **displayed** so as to perform automatic tracking. Since the celestial body which is to be brought in is **displayed** on the **display** 9, the star chart on the display 9 is shown to an observer to allow him to study even when the stars are not brought in the telescope 3 because of the changeableness of weather.

12/9/4 (Item 1 from file: 350)

010213780 **Image available**
WPI Acc No: 1995-115034/ **199515**
XRPX Acc No: N95-090798

Fault tolerant cross-channel computer data link forming ring network - uses partic. protocol in which optical **data of two discrete wavelengths are fed through single** optical **fibre, travelling clockwise and anticlockwise in two recurring time frames**

Patent Assignee: HONEYWELL INC (HONE)
Inventor: GOOSSEN E R; NELSON L A; WOODS J W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5396357	A	19950307	US 94187420	A	19940125	199515	B

Priority Applications (No Type Date): US 94187420 A 19940125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5396357	A		9	H04B-010/20	

Abstract (Basic): US 5396357 A

The cross-channel data link which provides communication between a number of computing elements of a fault tolerant **computing system** , has a multiplicity of nodes interconnected in a ring configuration. Each node is **coupled** to a **clockwise** adjacent node via a single **optical** fibre, and to a counterclockwise adjacent node via a different single **optical** fibre, and each node is coupled to one of the computing elements.

The nodes each include a first and second **optical** transmitter, and a first and second **optical** receiver. A first wavelength division multiplexer is coupled to the first **optical** transmitter and the first

METHOD FOR ALIGNING **OPTICAL** AXES OF SENSOR **MODULE** FOR DISTANCE **MEASUREMENT**

PUB. NO.: 59-003308 [JP 59003308 A]
PUBLISHED: January 10, 1984 (**19840110**)
INVENTOR(s): FUKUSHIMA YOSHIO
ONO YOSHIMI
APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-113737 [JP 82113737]
FILED: June 30, 1982 (19820630)
INTL CLASS: [3] G01C-003/00
JAPIO CLASS: 46.1 (INSTRUMENTATION -- Measurement); 29.1 (PRECISION INSTRUMENTS -- Photography & Cinematography)
JOURNAL: Section: P, Section No. 269, Vol. 08, No. 86, Pg. 154, April 19, 1984 (19840419)

ABSTRACT

PURPOSE: To improve the efficiency in aligning **optical** axes by turning an aperture member, which is disposed point-symmetrically with two openings of the same shape having an equal vertical angle so as to make the vertical angle coincident, by 1/2 of the vertical angle and measuring twice the output of a sensor **module** for distance **measurement** .

CONSTITUTION: An aperture plate 25 consists of a light-shieldable member provided with openings 26, 27 of the same sectorial shape having an equal vertical angle .theta. center-symmetrically so as to make the vertical angles coincident, and is used in superposition with a diffusion plate in the exit pupil position. The plate 25 is first mounted in the position where the axial line of the image of the cross aperture by a lenslet coincides with the X-axis. The output of an electric charge **coupling** element constituting photodetectors A(sub 1), B(sub 1),...A(sub 5), B(sub 5) is observed and the average value on the side A and B of the photodetectors is read. A sensor module 11 is adjusted around the X-axis until both average values are made equal. The plate 25 is rotated by .theta./2 **clockwise** , and the adjustment around the Y-axis is similarly accomplished.

17/9/7 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009219474 **Image available**
WPI Acc No: 1992-346896/ **199242**
XRPX Acc No: N92-264504
Measuring modules **sequential operator for banknote tester - responds to signal from transport device to initiate testing sequence defined by stored commands**
Patent Assignee: ANONYMOUS (ANON)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
RD 341018	A	19920910	RD 92341018	A	19920820	199242	B

Priority Applications (No Type Date): RD 92341018 A 19920820
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
RD 341018	A		1	G07D-000/00	

Abstract (Basic): RD 341018 A

The sequencer (1) is **coupled** to the microcomputer (3) and the memory (4) of the testing device via a first bus system (5), with a second bus system (6) for control and data signals between the sequencer (1) and each of the **measuring modules** (2.1...2.n). The sensors within the **measuring modules** (2.1...2.n) provide respective **optical** or magnetic analogue measured values, fed to a sensor circuit within the sequencer (1) via a number of signal lines (7.1,7.2,7.3). The sequencer (1) is operated in response to a signal from a transport device for the tested items. The commands for the testing sequence provided by the memory (4) with the testing cycle controlled via supplied **clock** signals, with the obtained measured signals transferred to a different segment (4.2) of the memory (4).

USE - For validity testing of banknotes.

Dwg.1/1

Title Terms: MEASURE; MODULE; SEQUENCE; OPERATE; BANKNOTE; TEST; RESPOND; SIGNAL; TRANSPORT; DEVICE; INITIATE; TEST; SEQUENCE; DEFINE; STORAGE; COMMAND

Derwent Class: T05

International Patent Class (Main): G07D-000/00

File Segment: EPI

Manual Codes (EPI/S-X): T05-J

17/9/8 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007983974 **Image available**

WPI Acc No: 1989-249086/ **198934**

XRPX Acc No: N89-189682

Closed loop fibre-optic gyroscope - phase modulates counter-propagating waves to lock phase difference alternately to values greater and less than that due to rotation

Patent Assignee: BERGH R A (BERG-I)

Inventor: BERGH R A

Number of Countries: 014 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8907237	A	19890810	WO 89US276	A	19890127	198934	B
US 4869592	A	19890926	US 88149140	A	19880127	198948	
EP 396632	A	19901114	EP 89904197	A	19890407	199046	
JP 3503568	W	19910808	JP 89503656	A	19890127	199138	
EP 396632	B1	19940713	EP 89904312	A	19890127	199427	
			WO 89US276	A	19890127		
DE 68916785	E	19940818	DE 616785	A	19890127	199432	
			EP 89904312	A	19890127		
			WO 89US276	A	19890127		
EP 396632	A4	19920715	EP 89904312	A	19890000	199522	

Priority Applications (No Type Date): US 88149140 A 19880127

Cited Patents: 1.Jnl.Ref; DE 3123163; DE 3244010

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8907237	A	E	43		
Designated States (National): JP KR					
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					
US 4869592	A		11		
EP 396632	A				
Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE					

20/9/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04545094 E.I. No: EIP96110399120
Title: Two-dimensional optical star-network
Author: Danzer, U.; Schwider, J.
Corporate Source: Universitaet Erlangen-Nuernberg, Erlangen, Ger
Conference Title: Proceedings of the 1996 Conference on Lasers and Electro-Optics Europe, CLEO/Europe
Conference Location: Hamburg, Ger Conference Date: 19960908-19960913
Sponsor: European Physical Society; Quantum Electronics & Optics Division ; IEEE/LEOS; Optical Society of America; Eur Optical Society
E.I. Conference No.: 45465
Source: Conference on Lasers and Electro-Optics Europe - Technical Digest 1996.. p 276 CThI50
Publication Year: 1996
CODEN: 85PNA9
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 9612W5
Abstract: An interconnection network for a modular expandable multiprocessor system is shown. Such a **computer system** needs a direct **coupling** among all processor units. For synchronization purposes or **clock** distribution the signal delay from one transmitter to all receivers should be the same. A fiber **optical** star network ensures a data distribution from all emitters to all receivers without delay, assuming equal fiber lengths. For this application, a star-topology bus system (STBS) has been developed. 2 Refs.
Descriptors: Fiber optic networks; Fiber optics; Diffraction gratings; Electric network topology; Transmitters; Signal receivers; **Optical** fiber coupling; Optoelectronic devices; Interconnection networks; **Optical** beam splitters
Identifiers: **Optical** star network; Star topology bus system; Free space **optical** setup; Wavelength
Classification Codes:
741.1.2 (Fiber Optics)
741.1 (Light/Optics); 741.3 (Optical Devices & Systems); 716.1 (Information & Communication Theory); 717.2 (Optical Communication Equipment); 722.4 (Digital Computers & Systems)
741 (Optics & Optical Devices); 716 (Radar, Radio & TV Electronic Equipment); 717 (Electro-Optical Communications); 722 (Computer Hardware)
74 (OPTICAL TECHNOLOGY); 71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

20/9/2 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01808119 ORDER NO: AADAA-I9937167
Multimode wavelength division multiplexing and demultiplexing using substrate-guided waves and volume holographic gratings
Author: Zhou, Chuang
Degree: Ph.D.
Year: 1998
Corporate Source/Institution: The University of Texas at Austin (0227)
Supervisor: Ray T. Chen
Source: VOLUME 60/07-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 3482. 124 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL ; PHYSICS, OPTICS
Descriptor Codes: 0544; 0752
ISBN: 0-599-38481-6

Wavelength division multiplexing and demultiplexing (WDDM) are considered key technologies to enhance the fiber optic transmission bandwidth. **Optical** communication systems based on WDDM technologies not only provide high speed data paths, but also provide the convenience of channel independence and data format transparency. I have designed and fabricated the first multi-mode WDDM based on axial graded index (AGRIN) lenses in conjunction with substrate-guided waves and a volume holographic grating. The diffraction-limited AGRIN lenses employed significantly increase the output coupling efficiency and reduce crosstalk when compared with the best homogeneous lens solutions previously reported. An active packaging strategy is effectively implemented and verified.

In high performance multi-chip-modules (MCMs), local area networks (LANs) and massive parallel processors (MPPs), connections among different chip elements are critical. Since for a massive parallel high performance computing, both the internal **clock** rate of the processor and the **connection** speed **determine** the **system** performance. Self-routing and non-blocking crossbar switches are ideal for such applications. Electronic switches, though easy to construct, are susceptible to RC delay. With increasing transmission rate and distance, the large resistance and capacitance will eventually limit the system speed to the connection speed. Building non-blocking and self-routing crossbar switches with optics is a natural choice for high performance parallel processing systems. Crossbar-based **optical** interconnection represents the most desirable network switching configuration due to its fast switching speed and low latency in transmitting high speed signals. In this dissertation, I present two types surface-normal non-blocking all **optical** crossbar interconnect based on surface-normal holograms. A prototype polymer-based 4 x 4 crossbar is experimentally demonstrated at 750, 780, 810 and 840 nm. The unique wavelength demultiplexing and beam routing properties of the volume holograms, in combination with the WDDM, reduce the required sixteen wavelengths to four wavelengths while maintaining the required sixteen (4 x 4) individual interconnects. Furthermore, the elimination of edge coupling significantly enhances the packaging reliability.

20/9/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07302792 **Image available**
METHOD AND SYSTEM FOR AUTOMATICALLY AVOIDING TIMING LOOP

PUB. NO.: 2002-171272 [JP 2002171272 A]
PUBLISHED: June 14, 2002 (20020614)
INVENTOR(s): KUNINOBE KANEI
APPLICANT(s): NEC CORP
APPL. NO.: 2000-364323 [JP 2000364323]
FILED: November 30, 2000 (20001130)
INTL CLASS: H04L-012/437; H04B-010/00; H04B-010/02; H04B-010/20; H04J-003/00; H04L-007/00; H04L-012/24; H04L-012/26; H04L-029/14; H04L-007/08

ABSTRACT

PROBLEM TO BE SOLVED: To provide an **optical** transmission communication device which automatically avoids a timing loop in an SDH network ring.

SOLUTION: When detecting a fault of an external clock signal generation device which generates a clock signal of the SDH network, the **optical** transmission communication device to which the external clock signal generation device is connected inserts fault information to OH in an SDH frame to report it to all **optical** transmission communication devices. Each **optical** transmission communication device receives fault information to judge whether the external clock signal generation device is connected to the device itself or nor. If the device is connected there, priority information is transmitted to a priority determination part from a device setting part where priority of the devices is stored, and the priority determination part receives this information to determine an external clock signal generation device, which should generate the clock signal of the SDH network, by priority information, and the **optical** transmission communication device to which the external **clock** signal generation **device determined** by the priority determination part is **connected** transmits the **clock** signal to the SDH network.

20/9/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010676458 **Image available**
WPI Acc No: 1996-173412/199618
XRPX Acc No: N96-145663
Optical **signal polarisation modulating appts. for communication system - has** clock coupled **to polarisation modulator and having frequency which** determines **frequency of** modulation **cycle with** clock **frequency locked and equal to predetermined frequency**
Patent Assignee: AT & T CORP (AMTT); TYCO SUBMARINE SYSTEMS LTD (TYCO-N); AMERICAN TELEPHONE & TELEGRAPH CO (AMTT)
Inventor: BERGANO N S
Number of Countries: 011 Number of Patents: 014
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 704996	A1	19960403	EP 95306638	A	19950920	199618	B
AU 9532840	A	19960418	AU 9532840	A	19950925	199623	
JP 8111662	A	19960430	JP 95248192	A	19950927	199627	
CA 2156759	A	19960328	CA 2156759	A	19950823	199628	
US 5526162	A	19960611	US 94312848	A	19940927	199629	
MX 9504059	A1	19970201	MX 954059	A	19950922	199818	
US 5912755	A	19990615	US 94312848	A	19940927	199930	
			US 96600102	A	19960208		
AU 9964401	A	20000302	AU 9532840	A	19950925	200021	N
			AU 9964401	A	19991209		
US 6057950	A	20000502	US 94312848	A	19940927	200029	
			US 96600102	A	19960208		
			US 99248192	A	19990209		
CA 2156759	C	20000627	CA 2156759	A	19950823	200043	
MX 191804	B	19990421	MX 954059	A	19950922	200055	
EP 704996	B1	20020327	EP 95306638	A	19950920	200222	
DE 69526019	E	20020502	DE 626019	A	19950920	200237	
			EP 95306638	A	19950920		
AU 746848	B	20020502	AU 9532840	A	19950925	200238	N
			AU 9964401	A	19991209		

Priority Applications (No Type Date): US 94312848 A 19940927; US 96600102 A 19960208; AU 9964401 A 19991209; US 99248192 A 19990209

Cited Patents: 2.Jnl.Ref; EP 361150
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 704996	A1	E	9	H04B-010/135	
Designated States (Regional): DE FR GB IT NL SE					
AU 9532840	A			H04B-010/145	
JP 8111662	A		9	H04B-010/00	
CA 2156759	A			H04B-010/145	
US 5526162	A		10	H04B-010/04	
MX 9504059	A1			H03C-001/00	
US 5912755	A			H04B-010/04	Cont of application US 94312848 Cont of patent US 5526162
AU 9964401	A			H04B-010/18	Div ex application AU 9532840
US 6057950	A			H04B-010/04	Cont of application US 94312848 Cont of application US 96600102 Cont of patent US 5526162 Cont of patent US 5912755
CA 2156759	C	E		H04B-010/145	
MX 191804	B			H04B-010/004	
EP 704996	B1	E		H04B-010/135	
Designated States (Regional): DE FR GB IT NL SE					
DE 69526019	E			H04B-010/135	Based on patent EP 704996
AU 746848	B			H04B-010/18	Div ex application AU 9532840 Previous Publ. patent AU 9964401

Abstract (Basic): EP 704996 A

The appts. includes a polarisation modulator which receives an **optical** signal onto which data has been modulated at a predetermined frequency. A clock, coupled to the polarisation modulator, has a frequency that determines the frequency of the modulation cycle. The frequency of the clock is phase locked and equal to the predetermined frequency.

The polarisation modulator modulates the state of polarisation of the **optical** signal at the predetermined frequency with a prescribed phase. An electrical variable-delay line couples the clock to the modulator for selectively varying the prescribed phase.

USE/ADVANTAGE - E.g. undersea or transcontinental lightwave transmission systems. Reduced signal fading for maintenance of good S/N ratio.

Dwg.1/5

Abstract (Equivalent): US 5526162 A

An apparatus for transmitting an **optical** signal comprising:

an **optical** signal source for generating an **optical** signal onto which data is modulated at a predetermined frequency;

a polarization modulator coupled to the **optical** signal source for modulating the state of polarization of the **optical** signal by tracing the polarization of said **optical** signal along at least a portion of a Poincare sphere such that an average value of the state of polarization over a modulation cycle is substantially equal to zero; and

a clock coupled to the polarization modulator having a frequency that determines the frequency of the modulation cycle, said frequency of the clock being phase locked and equal to said predetermined frequency.

Dwg.2/5

Title Terms: **OPTICAL** ; SIGNAL; POLARISE; MODULATE; APPARATUS; COMMUNICATE; SYSTEM; CLOCK; COUPLE; POLARISE; MODULATE; FREQUENCY; DETERMINE; FREQUENCY; MODULATE; CYCLE; CLOCK; FREQUENCY; LOCK; EQUAL; PREDETERMINED; FREQUENCY

Derwent Class: P81; V07; W02

International Patent Class (Main): H03C-001/00; H04B-010/00; H04B-010/004; H04B-010/04; H04B-010/135; H04B-010/145; H04B-010/18

International Patent Class (Additional): G02F-001/01; G02F-002/00; H03C-007/04; H04J-014/06
File Segment: EPI; EngPI
Manual Codes (EPI/S-X): V07-K02; V07-K03; W02-C04A1A; W02-C04A1X; W02-C04A7; W02-C04B1A

20/9/5 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009046471 **Image available**
WPI Acc No: 1992-173842/199221
XRPX Acc No: N92-130934
Optical **data storage discs test device - has output of preamplifier connected to subtraction input of first differential amplifier**
Patent Assignee: PENZA MATHEMATICAL MACH RES INST (PEMA-R); PENZA POLY (PEPO)
Inventor: BOGATYREV V G; KONNOV N N; KUCHIN A V
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SU 1658207	A1	19910623	SU 4719054	A	19890718	199221	B

Priority Applications (No Type Date): SU 4719054 A 19890718
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SU 1658207	A1		9	G11B-007/26	

Abstract (Basic): SU 1658207 A
The beam of laser light reflected off the surface of the tested disc (2) is picked up by an **optical** system (5) and then directed on to a photocell (6) whose output electrical signal enters a preamplifier (7). The latter's 'S' output signal contains the l.f. component and 'blips' residing in the h.f. part of the signal spectrum, which characterise the local flaws in the disc such as scratches and inclusions on the reflective coating and base of the disc. To test for local defects in the disc, and the coefft. of reflection from the disc, the signal from the preamp. (7) is fed into a low-pass filter (8) for extracting the h.f. component, i.e. signal S H.CH. Better test fidelity and productivity are claimed by using the low-pass filter (8), together with first and second differential amplifiers, controlled reference voltage source, first and second reference voltage sources, registering unit **clock** pulse generator, **computation device** and by having the disc rotation drive **joined** to the tested disc. The output of the pre-amp. (7) is connected to the subtracting input of the first differential amplifier.
USE - Data storage engineering. Bul.23/23.6.91.
Dwg.1/5
Title Terms: **OPTICAL** ; DATA; STORAGE; DISC; TEST; DEVICE; OUTPUT; PREAMPLIFIER; CONNECT; SUBTRACT; INPUT; FIRST; DIFFERENTIAL; AMPLIFY
Derwent Class: T03; W04
International Patent Class (Main): G11B-007/26
International Patent Class (Additional): G01B-021/30
File Segment: EPI
Manual Codes (EPI/S-X): T03-B; W04-C
?

24/9/16 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008763926 **Image available**
WPI Acc No: 1991-267939/ **199137**
XRPX Acc No: N91-204593
Synchronising clocks **in loosely** coupled , **distributed** computer system **- triggering number of microcomputers contg. local clocks from central microcomputer**
Patent Assignee: DEUTS REICH WISS TE (DERE-N)
Inventor: PALACIOS S; ROSENDAHL D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DD 289147	A	19910418	DD 343801	A	19891108	199137	B

Priority Applications (No Type Date): DD 334380 A 19891108; DD 343801 A 19891108

Abstract (Basic): DD 289147 A
The method of synchronising clocks in a loosely coupled, distributed microcomputer system consisting of a communications system and a number of microcomputers contg. local clocks involves triggering from a central microcomputer. Time messages contg. date and time are formed in its central clock and sent to distributed microcomputers. Their local clocks are set according to known algorithms after properly acknowledged receipt of the time message and they pass the message on to further microcomputers where the **process** is repeated.
USE/ADVANTAGE - For distributed system contg. microcomputers functioning as node computers or data stations. Clock synchronisation is improved without using additional circuits or synchronisation units.
(4pp Dwg.No.1/1
Title Terms: SYNCHRONISATION; CLOCK; LOOSE; COUPLE; DISTRIBUTE; COMPUTER; SYSTEM; TRIGGER; NUMBER; MICROCOMPUTER; CONTAIN; LOCAL; CLOCK; CENTRAL; MICROCOMPUTER
Derwent Class: T01
International Patent Class (Additional): G06F-015/16
File Segment: EPI
Manual Codes (EPI/S-X): T01-H07B; T01-J02A; T01-K

24/9/17 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008746732 **Image available**
WPI Acc No: 1991-250748/ **199134**
XRPX Acc No: N91-190918
Digital filter for discrete fourier transform - has synchroniser with two clock outputs connected **to second and third** clock inputs **of** calculation module
Patent Assignee: ZHITOMIR KIEV POLY (KIPO)
Inventor: KANEVSKII Y U S; KONOPLITSK I A; KORCHEV D V
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SU 1596347	A	19900930	SU 4603585	A	19881109	199134	B

Priority Applications (No Type Date): SU 4603585 A 19881109

Abstract (Basic): SU 1596347 A

The device includes data **input** , **input** memory, commutator, data rail, ROM, N flipflops (N - length of pulse characteristic), AND-gates, NOT-gates, **input** registers, multipliers, adders, output registers, accumulator, constant component output, wt. coeffts. output, synchroniser, clock pulse generator, output memory, delay unit, harmonics output, calculation modules, commutators and filtering output.

USE/ADVANTAGE - In computer engineering, e.g. for discrete Fourier transform and digital filtering, partic. in digital signals **processing** . Simplified design. Bul.36/30.9.90. (7pp Dwg.No.1/5)

Title Terms: DIGITAL; FILTER; DISCRETE; FOURIER; TRANSFORM; SYNCHRONISATION ; TWO; CLOCK; OUTPUT; CONNECT; SECOND; THIRD; CLOCK; **INPUT** ; CALCULATE; MODULE

Derwent Class: T01

International Patent Class (Additional): G06F-015/35

File Segment: EPI

Manual Codes (EPI/S-X): T01-J04

24/9/18 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

008687430

WPI Acc No: 1991-191449/ **199126**

Related WPI Acc No: 1992-206596

XRPX Acc No: N91-146447

Computer subscriber to common bus interface - has first input **of fourth OR-gate acting as end of transmission subscriber output signal**

Patent Assignee: PERM PARMA PRD ASSC (PRPA-R)

Inventor: KAYUSHEV E V; KISELEV V I; POPOV V N

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SU 1583936	A	19900807	SU 4445470	A	19880621	199126	B

Priority Applications (No Type Date): SU 4445470 A 19880621

Abstract (Basic): SU 1583936 A

The interface includes matching units (1,2), selector (3), address register (4), address counter (5), shift registers (6,7), counters (8-10), flipflops (11-14), AND-gates (15-17), OR-gates (18-20), delay elements (21-23) and NOR-gate (25). A pulse from the start rail (38) independent to status of bus (26) sets fifth flip flop (36) allowing the content of the shift register (7) to be transferred into the bus (26) via OR-gate (37), NOR-gate (25) and second matching element (2).

USE/ADVANTAGE - In computer engineering, e.g. distributed **computer systems** contg. several **clock** data sources **connected** to data bus. Improved fidelity of operation and wider functional scope. Bul.29/7.8.90.

Dwg.1/1

Title Terms: COMPUTER; SUBSCRIBER; COMMON; BUS; INTERFACE; FIRST; **INPUT** ; FOURTH; OR-GATE; ACT; END; TRANSMISSION; SUBSCRIBER; OUTPUT; SIGNAL

Derwent Class: T01

International Patent Class (Additional): G06F-013/00

File Segment: EPI

immunity to interference and the phase stability. Bul.21/7.6.88.
(4pp Dwg.No.1/2
Title Terms: PHASE; STABILISED; CLOCK; SYNCHRONOUS; PULSE; SHAPE; AMPLITUDE ; DETECT; **INPUT** ; SEC; WIND; OUTPUT; OR-GATE
Derwent Class: U22
International Patent Class (Additional): H03K-005/01
File Segment: EPI
Manual Codes (EPI/S-X): U22-D01

24/9/24 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007101367
WPI Acc No: 1987-101364/ **198714**
XRPX Acc No: N87-076178
BPSK synchroniser using computational analysis - repetitively samples amplitude of input **signal over preselected sampling interval portion of each modulating signal bit period**
Patent Assignee: FORD AEROSPACE & COMMUNIC CORP (FORD)
Inventor: WISNIEWSKI J H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4653075	A	19870324	US 85717999	A	19850329	198714	B

Priority Applications (No Type Date): US 85717999 A 19850329
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4653075	A		16		

Abstract (Basic): US 4653075 A
The appts. has a device for taking several samples of the amplitude of the **input** signal over a sampling interval portion of each modulating signal bit period. The frequency f is an integral multiple of the rate at which the sampler samples the amplitude of the **input** signal. Coupled to the sampler a device records for each sampling interval, the total number of samples, the number of samples that change sign w.r.t. a reference sample, and the number of samples that do not change sign w.r.t. the reference sample.
Coupled to the recorder a device determines a synchronisation condition when, within a sampling interval, the number of samples which have been recorded not to have changed sign exceeds a preselected threshold level. **Coupled** to the **determining device** a **device** generates an output **clock** synchronised with the modulated **input** signal, and having a frequency equal to the modulating signal bit rate, when the determining device has determined a synchronisation condition.
5/5
Title Terms: SYNCHRONISATION; COMPUTATION; ANALYSE; REPEAT; SAMPLE; AMPLITUDE; **INPUT** ; SIGNAL; PRESELECTED; SAMPLE; INTERVAL; PORTION; MODULATE; SIGNAL; BIT; PERIOD
Derwent Class: W01
International Patent Class (Additional): H04L-007/02
File Segment: EPI
Manual Codes (EPI/S-X): W01-A04; W01-A09B

24/9/25 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

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007020864
WPI Acc No: 1987-020861/ **198703**
XRPX Acc No: N87-015718
Electro-musical instrument scale frequencies generator - has output of clock pulse generator connected to clock input of computing device
Patent Assignee: PARTALA O N (PART-I)
Inventor: PARTALA O N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SU 1234878	A	19860530	SU 3792971	A	19840920	198703	B

Priority Applications (No Type Date): SU 3792971 A 19840920
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SU 1234878	A		5		

Abstract (Basic): SU 1234878 A

The generator includes series-connected clock pulse generator (1) and counter (2), and also an adder (3) and a computing device (4), a memory unit (5), pulse distributor (6) and a delay unit (7). The inclusion of the memory unit (5), pulse distributor (6) and delay unit (7) allows simultaneous generation of frequencies for all types of musical instruments thus extending the functional scope of the generator.

USE/ADVANTAGE - Electronic musical instruments, i.e. generation of scale frequencies. Improved operating reliability by reducing number of components and circuitry. Bul.20/30.5.86. (5pp Dwg.No.1/3)

Title Terms: ELECTRO; MUSIC; INSTRUMENT; SCALE; FREQUENCY; GENERATOR; OUTPUT; CLOCK; PULSE; GENERATOR; CONNECT; CLOCK; **INPUT** ; COMPUTATION; DEVICE
Derwent Class: P86; W04
International Patent Class (Additional): G10H-001/00
File Segment: EPI; EngPI
Manual Codes (EPI/S-X): W04-U01

24/9/26 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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004143935
WPI Acc No: 1984-289475/ **198447**
XRPX Acc No: N84-215876
Computer controlled clock monitoring equipment - uses capacitive monitors on clock dials connected to multivibrators and computerised frequency measuring system
Patent Assignee: FORSCH UHREN & FEIN (UHRE-N)
Inventor: BADERSCHNE K
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3317463	A	19841115	DE 3317463	A	19830513	198447	B
DE 3317463	C	19850523				198522	

Priority Applications (No Type Date): DE 3317463 A 19830513
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
DE 3317463 A 14

Abstract (Basic): DE 3317463 A

The method of monitoring more than one clock uses a capacitative measuring system in which sensors are incorporated in the dial of each clock, adjacent to the hour, minute and second hands. Each sensor forms an electrical connection and is attached by an insulated support, being capacitatively connected to a multivibrator whose frequency is inversely proportional to the capacity. A multiplexing system is used with a frequency counter so that the frequencies are measured at time intervals.

The measured values are stored and differences monitored and programmed to operate a switching system. The dial of the clock is divided into sectors which are scanned according to a programmed computer system, and the scanning signals are stored in a memory. The monitoring signals can be used to operate an acoustic device which can e.g. produce a time.

USE - The system may be used for time **indication** or for time correction.

0/2

Abstract (Equivalent): DE 3317463 C

The contactless position measuring system for the position of the hands of an analog clock enables a striking system or contacts for control purposes to be operated. The clock face is divided into zones so that the capacity can be used to operate multivibrators. They are operated so that their frequency is changed inversely according to the measured capacitance.

A multiplexing system is used with a frequency counting system in which measurements are made at time intervals and stored in a memory, for comparison with programmed values. The comparison signals are used to operate switching circuits which supply the control signals.

ADVANTAGE - More compact than system using coding discs. (7pp)

Title Terms: COMPUTER; CONTROL; CLOCK; MONITOR; EQUIPMENT; CAPACITANCE; MONITOR; CLOCK; DIAL; CONNECT; MULTIVIBRATOR; COMPUTER; FREQUENCY; MEASURE; SYSTEM
Derwent Class: S02; S04
International Patent Class (Additional): G01D-013/26; G04C-009/00; G04C-021/00; G04G-009/00; H03K-013/18
File Segment: EPI
Manual Codes (EPI/S-X): S02-K06A; S04-B03; S04-B04; S04-B05

24/9/27 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003739415
WPI Acc No: 1983-735612/ **198333**
XRPX Acc No: N83-141845
Incremental distance measuring system - has clock generator driving two interconnected frequency dividers
Patent Assignee: SCHLEICHER S (SCHL-I)
Inventor: SUESS M
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
DD 200375 A 19830420 198333 B

Priority Applications (No Type Date): DD 232827 A 19810827
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
DD 200375 A 13

Abstract (Basic): DD 200375 A

The distance-measuring system contains a **processing** circuit that generates a reference pulse sequence and compares this sequence with the sequence of measured pulses resulting from the measurement of distance. A clock generator feeds two frequency dividers. The stage outputs from the first divider (6) are connected to the set **inputs** of the corresponding stages of the second divider (7).

The set **inputs** of the second divider are actuated by a zero-pulse generator (4). The actual distance- **measuring device** (1) is **connected** to the **clock** generator (8) for synchronisation. A pulse summation circuit (5) combines outputs from the distance-measuring device and the clock generator for applying to the second divider.

1/3

Title Terms: INCREMENT; DISTANCE; MEASURE; SYSTEM; CLOCK; GENERATOR; DRIVE; TWO; INTERCONNECT; FREQUENCY; DIVIDE
Derwent Class: S02
International Patent Class (Additional): G01D-005/24
File Segment: EPI
Manual Codes (EPI/S-X): S02-A02A; S02-K03A2; S02-K03A9

24/9/28 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003722014
WPI Acc No: 1983-718206/ **198330**
XRPX Acc No: N83-128418

Talking clock speech generator - has noise suppressor with logic circuit blocking clock pulse generator during power supply interruption

Patent Assignee: SHARP KK (SHAF)
Inventor: NISHIMURA K; NITTAYA H
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3300231	A	19830721	DE 3300231	A	19830105	198330	B
US 4564954	A	19860114	US 83455769	A	19830105	198605	
DE 3300231	C	19860424				198618	

Priority Applications (No Type Date): JP 822027 A 19820108
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
DE 3300231 A 11

Abstract (Basic): DE 3300231 A

The speech synthesis **device** for talking **clocks** , **calculators** , etc. has a central **processing** unit **connected** to an **indicator** and to operating buttons, and is connected to a speech generator. The speech generator incorporates a crystal controlled oscillator forming a basic clock pulse generator. The circuit includes a switch for interrupting the power supply when speech is not being generated and a noise suppression system.

A logic circuit incorporated in the speech generator disconnects the clock pulse generator and is blocked before a fault can be cuased by the interruption in the power supply. The clock pulse generator has **input** and output capacitors which determine the operating conditions, the value of one of the capacitors being selected to ensure that the

voltage of the oscillations is greater than the level for faulty operation of the logic circuit.

Abstract (Equivalent): US 4564954 A

The device includes at least a speech synthesiser, a power amplifier, a logic circuit, and an oscillator for providing a fundamental clock signal. An arrangement is provided for interrupting power to the speech generator when speech generation is not being performed. The logic circuit is stopped by controlling and stopping the fundamental clock oscillator of the speech synthesiser before the logic circuit malfunctions due to a drop in power supply voltage when power to the synthetic speech generator is interrupted.

The stopping arrangement is forcibly executed in relation to power supply interrupt commands to the synthetic speech generator. The oscillator comprises capacitors to establish an oscillation condition, the capacitance of one of these being set so that it will oscillate at a voltage higher than that which causes a malfunction of the logic circuit.

ADVANTAGE - Eliminates noise generated each time speech communication is completed. (5pp)1

Title Terms: TALK; CLOCK; SPEECH; GENERATOR; NOISE; SUPPRESS; LOGIC; CIRCUIT; BLOCK; CLOCK; PULSE; GENERATOR; POWER; SUPPLY; INTERRUPT

Derwent Class: P86; S04; T01; W02; W04

International Patent Class (Additional): G06F-003/16; G10L-001/10; G10L-003/00; H04B-015/02

File Segment: EPI; EngPI

Manual Codes (EPI/S-X): S04-B05; T01-C09; W02-H; W04-V

24/9/29 (Item 22 from file: 350)

DIALOG(R)File 350:Derwent WPIX

003321730

WPI Acc No: 1982-G9744E/ **198224**

Processor **quartz clock synchronisation control - detects time keeping relative to master clock to switch between different quartz circuits**

Patent Assignee: BBC BROWN BOVERI & CIE AG (BROV)

Inventor: HECHT S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3042808	A	19820609				198224	B

Priority Applications (No Type Date): DE 3042808 A 19801113

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3042808	A		10		

Abstract (Basic): DE 3042808 A

The synchronisation control for **processor** clocks in a decentralised multiprocessor system uses a timing deviation **measuring device coupled** to the respective **processor clock** and to the master clock. Its output controls a selection switch allowing one of several alternate quartz circuits with differing frequencies to be coupled to the clock so as to reduce the detected timing deviation.

Pref. each quartz circuit is coupled to the selection switch via an oscillation monitor for synchronising the change-over. The synchronisation control is used for clocks incorporated in **processors** spaced at wide distances.

Title Terms: **PROCESSOR** ; QUARTZ; CLOCK; SYNCHRONISATION; CONTROL; DETECT;

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Set     Items   Description
S1    1893874   (MEASUR? OR CALCULAT? OR COMPUT? OR DETERMIN? OR EVALUAT?)-
             (3N)(DEVIC? OR SYSTEM? OR APPARATUS? OR MODUL?)
S2     366164   CLOCK? OR WATCH? ?
S3   10420419   PROCESS???? OR MICRO()PROCESSOR? OR MICROPROCESSOR?
S4    9370625   INPUT? ? OR INDICAT? OR POINT??? OR DISPLAY?
S5    8246985   COUPL??? OR CONNECT???? OR ATTACH? OR JOIN????
S6    4085479   OPTICAL? OR WIRELESS? OR INFRARED OR NON()GALVANIC? OR NON-
            GALVANI? OR NON()TOUCH? OR NONTOUCH?
S7       5901   S5 AND S1 AND S2
S8        403   S5(10N)S1(10N)S2
S9        269   S8 AND (S3 OR S4)
S10        12   S9 AND S6
S11         8   S10 AND PY<=1997
S12         8   RD (unique items)
S13     37253   MEASUR?(3N)MODUL?
S14        71   S13 AND S5 AND CLOCK?
S15        15   S14 AND S6
S16        15   S15 NOT S12
S17         9   S16 AND PY<=1997
S18    319422   CLOCK? ? OR WATCH? ?
S19       200   S1(6N)S18(6N)S5
S20         5   S6 AND S19
S21        77   S1(3N)S18(3N)S5
S22        44   S21 AND PY<=1997
S23        44   S22 NOT (S12 OR S17 OR S20)
S24        33   S23 AND (S3 OR S4)
?  show files
File   2:INSPEC 1969-2003/Apr W2
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